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RN-6765

B. E. - III (Sem. V) (Computer) Examination

May / June – 2010

Microprocessors & Interfacing Techniques

Time : **3** Hours] [Total Marks : **100**

Instruction :

નીચે દર્શાવેલ ☛ નિશાનીવાળી વિગતો ઉત્તરવહી પર અવશ્ય લખવી.
Fillup strictly the details of ☛ signs on your answer book.

Name of the Examination :

☛ B. E. - 3 (Sem. 5) (Computer)

Name of the Subject :

☛ Microprocessors & Interfacing Techniques

☛ Subject Code No. : 6 7 6 5 ☛ Section No. (1, 2,.....) : 1&2

Seat No. :

Student's Signature

SECTION - I

1 (a) Answer the following : **10**

(i) The 8085 microprocesor can access memory location upto _____H.

(ii) _____ A logical instruction sets Z (zero) flag, but contents of Accumulator are unaffected.

(iii) _____ instruction must be used to transfer the contents of Accumulator to memory location specified by HL register pair.

(iv) If the result of an arithmetic instruction is 00H is Accumulator, the Z (zero) flag = 0. (True/false)

(v) Mention the number of Machine Cycles and T-states for the 8085 instruction : LXI.

(vi) Mention the nuber of Machine Cycles and T-states for the 8085 instruction : RAR.

(vii) An input port and an output port can have the same port address. – Justify.

(viii) Explain the function of pin : Ready.

(ix) Mention the four Peripheral or Externally Initiated operations to which 8085 μP can respond.

(x) What is power-on reset?

(b) Specify the addressing mode and explain the instructions with example. 4

(i) OUT

(ii) INX

(c) Answer the following questions : 6

(i) Write a routine HLSP that transfers the contents of SP to HL. No other registers in microprocessor should be affected.

(ii) Specify the number of times the following loop is executed.

```
    LXI B, 1000 H
LOOP : DCX B
    NOP
    JNZ LOOP
```

(iii) What is shadow memory?

2 (a) Draw and explain timing diagram of the following instruction. 7

C100 : STA 8040H

Opcode of STA : 32H

Draw waveform at all important pins.

(b) Write a program to calculate the squares of first N natural numbers. N is a 4 bit number stored at memory location C050H and output is stored at C051H onwards. 8

OR

(b) Write a program equivalent to the following c code : 8

```
for (i = 0; i < 10; i++)
    arr[i] = arr[i] * 2;
```

arr is stored at memory location C200H onwards.

3 (a) Interface 16K × 8 EPROM using 4K × 8 chips and one 8255 to 8085. Draw the neat diagram showing the interface scheme and clearly explain the memory map for both devices. Make necessary assumptions and explain with the help of necessary diagrams. **10**

(b) Show the contents of all affected registers (including PC and SP) as well as memory locations, after execution of each instruction in the following segment of program : **5**

```
4000 :  LXI SP, 2000 H
        LXI H, 3000 H
        PUSH H
        DCX H
        INR H
        POP B
```

OR

(b) What is the use of control signals in 8085 ? How control signals are generated? **5**

SECTION - II

4 (a) State true or False : **10**

(i) SPHL instruction can be used to load a new address in Stack pointer register.

(ii) TRAP interrupt has lower priority than HOLD signal for DMA.

(iii) A subroutine can have more than one Return statements.

(iv) RST instructions are 1-byte call instructions.

(v) Instruction DAA converts a binary number to BCD number.

(vi) ALE, IO/M', RD' WR' signals from 8085 can be directly connected to 8155 without the need of external demultiplexing of AD_0–AD_7 or generation of control signals.

(vii) In 8279, when A_0 is high(=1), signals are interpreted as data, else control word or status word.

(viii) 8155 includes 512 bytes of R/W memory.

(ix) Mode 2 of 8255 is known as Bidirectional data transfer mode.

(x) 8259 has one ISR (Interrput Service Register) to store all the pending interrupts.

(b) Attempt any **two** : **10**

(i) Give the flowcharts for Status Check I/O and Interrupt I/O.

(ii) Explain steps involved in DMA operation carried out by 8085 microprocessor system having 8257 DMA controller.

(iii) Explain with the help of diagram, data transfer during execution of CALL instruction.

5 (a) What is key bouncing? Explain hardware and software solutions for this problem. **8**

OR

(a) Explain all modes of 8254 in brief. **8**

(b) Draw the block diagram of 8259. Also list all features of 8259. **8**

6 (a) Explain the response 8085 to INTR interrupt request. Explain with proper diagram how external hardware can be used to provide code for interrupt type to 8085. **10**

(b) Explain RIM instruction with detail of each bit. **4**

OR

(b) Write a routine to enable all interrupts in an 8085 system. **4**